Robust Packaging Solution For DTT Magnetic Sensors

Semester Project - Final report
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Abstract

This project details the development of a robust packaging solution for DTT magnetic sensors in the context of the DEMO tokamak reactor for fusion energy. The process flow, detailing the first prototype, is shaped by microfabrication techniques and expert insights, prioritizes choices like wet etching and a double-layer mask for glass etching. Challenges encountered offer valuable lessons for future projects. Clear steps for completion, including inspections, bonding experiments, and coil integration, are outlined. The findings contribute to materials processing knowledge for fusion reactor applications, providing insights for researchers and paving the way for future advancements.

Contents

1 Introduction

Energy is crucial for societal development, and as global demand rises, exploring sustainable solutions becomes imperative. Fossil fuels pose environmental challenges, prompting a need for cleaner alternatives. Nuclear energy stands out, offering a potent, low-carbon option with consistent electricity generation. Despite challenges like safety and waste disposal, ongoing research and innovation address these concerns. Nuclear power, alongside renewables and efficiency measures, contributes to a diversified and sustainable energy landscape, supporting progress while minimizing carbon emissions.

One step in that direction is the DEMO tokamak reactor. It aims to connect to the grid, delivering electrical energy efficiently generated by fusion reactions. Fusion relies on a magnetic field to confine plasma, characterized by a complex 3D and time-varying topology. This field, encompassing quasi-static equilibrium and high-frequency fluctuations, necessitates precise measurement for fusion reaction control. For these reasons, robust and relaible magnetic sensors are pivotal for ensuring the success and viability of DEMO and, more broadly, advancing the practical application of fusion energy on a larger scale. Moreover, tokamak environment is challenging due to thermal radiation and neutron fluxes.

The overall goal is to enhance magnetic sensor design, originally developed with LTCC and HTCC since 2007, using recent microfabrication developments, particularly photo-lithography, to improve performance, compactness, and manufacturability. To do so, connection to in-vessel cabling is detrimental for seamless integration and effective operation within the tokamak environment.

The objective of this project is to develop a packaging solution to seamlessly connect sensors to the external world. The prototype should showcase enhanced connectivity and reliability, ensuring that the deposited tracks are well-protected and capable of measuring magnetic fields. This project also aims to leverage proprietary Impulse Current Bonding (ICB) techniques and connectors provided by a specialized Swiss company, Sy&Se.

2 Related Work

2.1 Research at the SPC

The researchers at the Swiss Plasma Center, EPFL, have achieved a notable milestone in the advancement of inductive magnetic sensor technology through the integration of photolithography techniques into the fabrication process. This strategic integration has enabled the deposition of tracks with more precision and efficiency, addressing the critical challenge of reducing track width (dd1) to below 10 μm, fostering the creation of highly compact and optimized sensor designs. The key achievement lies in the ability to accommodate more planar winding loops over a diminished geometric surface, thereby concurrently minimizing self-inductance (Lself). Moreover, the adaptability of the design for both high and low-frequency applications, contingent upon the manipulation of stacked-up layers (n), underscores the versatility conferred by the PL techniques.

They also have addressed the connection to in-vessel cabling. Traditional industrial wire-bonding techniques, typically employed for connecting thin wires, prove unsuitable in this context as the wires in question are less than a micrometer thick. Direct brazing, another commonly used method, is also deemed inappropriate due to the wafer's extreme sensitivity to highly localized thermal stresses. Moreover, standard anodic bonding techniques, widely applied for metal-to-glass sintering, have proven ineffective for the specific requirements of this innovative sensor technology .

This realization highlights the intricacies and unique challenges associated with the holistic development of inductive magnetic sensors, emphasizing the need for specialized solutions for packaging and encapsulation.

2.2 Literature review

Micro-coils serve as fundamental components or key features in a multitude of applications, showcasing their adaptability and importance across diverse fields.

An example of that would be implantable magnetic stimulation devices for therapeutic neurostimulation using MEMs technology. In terms of encapsulation, the micro-coils are designed utilizing aluminum oxide (Al2O3) and parylene C for electrical insulation, and are packaged using standard methods such as custom PCBs, gold wire bonding, epoxy glue sealing, and a parylene C coating [7].

Another application is the development of a lab-on-chip concept for highly efficient immunoassays. The traditional ones using magnetic nanoparticles (MNP) controlled by a permanent magnet are deemed unreliable or insufficient for fully integrated lab-on-chip systems. The integration of microcoils is explored to enhance the efficiency of immunoassays. This involves the bonding of microcoils onto a PCB board, and wire-bonding is performed using aluminum wire to establish electrical connections. The microcoils are then covered with a 10 μm PDMS layer for protection and preparation for O2 plasma bonding with the microfluidic channel part. The bonding process is facilitated through O2 plasma treatment, ensuring a strong and reliable connection between the microcoils and the microfluidic channels. The bonding conditions include a power of 160 W with an O2 pressure of 0.4 mbar and a duration of one

minute [6].

Flip-Chip bonding has proven to be a good technique as well, especially in the simulation and fabrication of micro-magnetometers [2]. The fabrication of the magnetometer involves a systematic process (See figure 11) that begins with a silicon substrate coated with sputtered aluminum. A photoresist layer is applied, and a UV light pattern transfer is executed. Etching selectively removes unwanted metal, shaping the coil. After stripping the photoresist, an insulating layer covers the microcoil. Simultaneously, the coil is again patterned and exposed in order to create the connector to establish an electrical connection between the microcoil and external circuitry. In the packaging stage, Flip-Chip bonding is utilized — an efficient assembly method where the microcoil is directly attached to another substrate using solder bumps. The controlled application of heat melts the solder, creating a secure bond between the microcoil and the target substrate. This method ensures a precise and compact connection, streamlining the packaging process.

The project at hand recognizes the existing challenges associated with the development and application of inductive magnetic sensors, particularly in the demanding environment of the DEMO tokamak reactor. The literature review reveals a range of applications, each presenting its own set of encapsulation and bonding techniques tailored to specific needs. The limitations of traditional wire-bonding, direct brazing, and standard anodic bonding techniques underscore the need for a specialized solution.

3 Methodology

3.1 Microfabrication of coils

The first weeks of the project involved fabricating and depositing gold and copper micro-coils on SiO2 and Sapphire wafers of 525 μm thickness (ss2) with the use of KLayout software. Pads measuring 3 mm x 3 mm were incorporated for electrical connections. The specifications for these micro-coils are as follows:

- Dimensions: $20\,\text{mm} \times 20\,\text{mm}$ for the height (h) and width (w) of one die, with 9 dice on a single wafer.
- Effective surface area (NA_{eff}): $10 \times 10^{-3}\,\text{m}^2$.
- Tracks dimensions: dd1 (width): 10 μm, ss1 (separation): 10 μm, dd2 (thickness): 500 nm

3.1.1 Calculation of Resistance and Self-Inductance

We define:

$$\begin{aligned} g &= 2\,(dd_1 + ss_1) \\ w' &= w - 2dd_1 \\ h' &= h - 2dd_1 \\ n &= 1\,(number\,of\,stacked - up\,coils) \\ m &\quad number\,of\,turns \end{aligned}$$

and:

$$\begin{aligned} A_{\text{eff}} &= n \sum_{i=0}^{m-1} (w' - ig)\,(h' - ig) \\ &= \frac{mn}{6}\left[g^2\left(2m^2 - 3m + 1\right) - 3g(m-1)\,(h' + w') + 6h'w'\right] \end{aligned} \tag{1}$$

Observing that m = 26 satisfies the equation for an effective surface area of $A_{\text{eff}} = 9.86 \times 10^{-3}\,\text{m}^2$

We define now the coil length l:

$$l = 20 + 2 \cdot \sum_{i=1}^{2m} (20 - i \cdot dd1 - (i-1) \cdot ss1) = 2.09m$$

We have:

$$L_{\text{self}} = \frac{4\pi \cdot \mu_0 \cdot A_{\text{eff}} \cdot (nm)^2}{\sqrt{4 \cdot l^2 + A_{\text{eff}}}}$$

and:

$$R = \rho\,\frac{l}{S}$$

so: R = $10.1k\Omega$ and $L_{\text{self}} = 2.51 \times 10^{-5}$ H

with :

$\rho = 2.44 \times 10^{-8}\Omega\cdot$ m and S = dd1 $\cdot$ dd2 = 5×10^{-12} m^2

3.2 Exchanges with M. Brun

The second part of the project consisted of understanding M. Brun's process flow (see Appendices 6) and adapt it to DTT magnetic sensors application.

M. Brun's silicon micromachining project aims to fabricate silicon components with the ultimate goal of achieving successful ICB for interconnections and packaging in the final device. It notably uses deep reactive ion etching (DRIE) on both sides of 4-inch silicon wafers, as this technique is well-suited for creating high aspect ratio structures and is capable of providing anisotropic etching on both sides simultaneously with precise control over etching depth, profile, and sidewall smoothness, as needed for this project. The process also involves key steps such as thermal oxidation, resist coating, photolithography, plasma stripping, and evaporation of a Ti-Al layer.

The initial prototype, illustrated in Figure 1, features a simplified track design deposited on a Si wafer with a layer of oxide. This design facilitates the alignment of two connection outputs, strategically positioned as holes etched through Deep Reactive Ion Etching (DRIE) and electrically linked to the tracks. To enhance the insulation properties and provide a suitable dielectric layer essential for subsequent Impulse Current Bonding (ICB) at Sy&Se, a TiO2 layer is sputtered across the entire wafer, excluding the connection holes. Notably, to optimize the bonding process, M. Brun recommended adopting a partial bonding approach. This involves creating a "Walls of Lucca" configuration—an enclosing rectangle around the tracks. This targeted structure ensures a more robust bonding and sealing process for improved control and efficiency. Finally, a wire will be inserted into the hole between the fused silica wafer and the counter-piece to connect the tracks to external components.

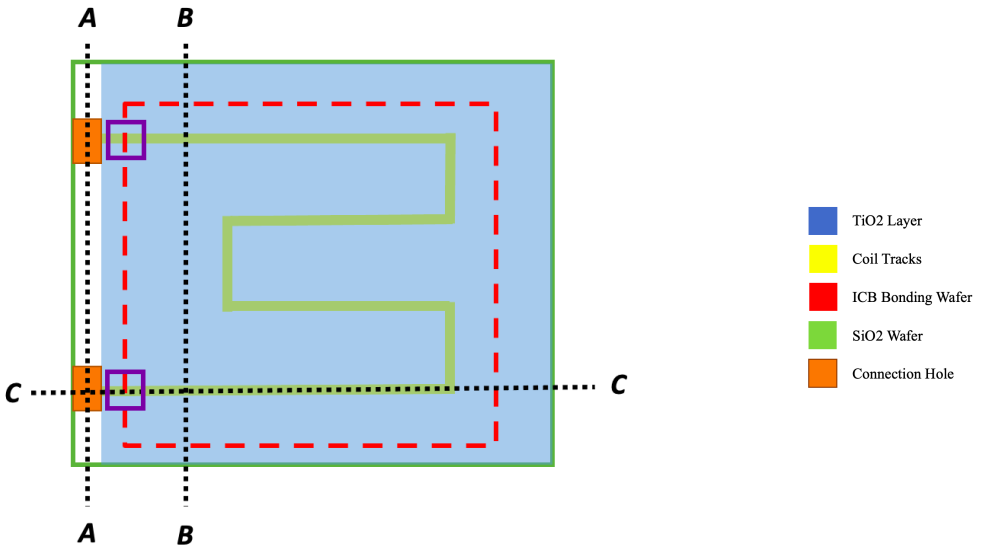


Figure 1: Top view of the prototype

Figure 2: Cross-section C-C

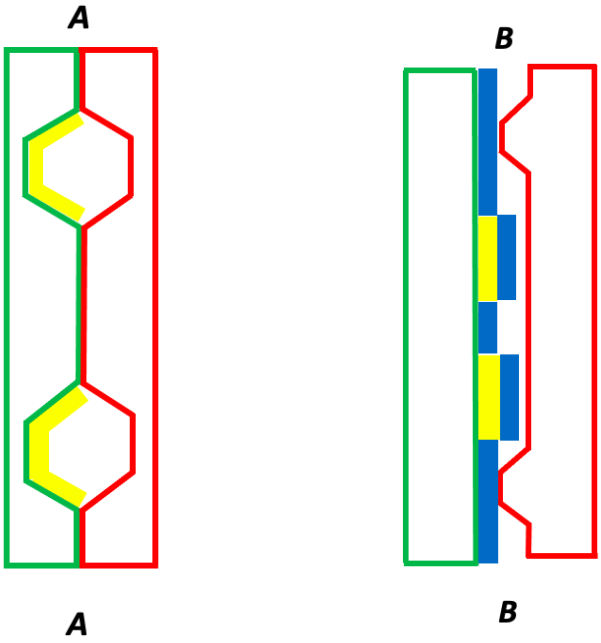


Figure 3: Cross-sections A-A and B-B

An additional critical consideration involves the counterpart component that will be affixed to the sensor substrate. Various materials are under consideration, with one suggested option being type JGS3 fused silica. Fused silica comes in three main types: JGS1, JGS2, and JGS3, ordered from the purest to the least pure, all available on University Wafers [4]. Opting for JGS3 can be advantageous due to its higher impurity content, which is essential for achieving effective anodic bonding. Alternatively, a TiO2 layer is another viable option. In cases where this proves ineffective, rather than bonding two TiO2 layers, another approach involves depositing a layer of Si over the TiO2 to serve as an insulating layer. The counterpiece should also be micro-machined, as illustrated in Figure 3.

Several questions have arisen concerning general feasibilities. One of them is determining the optimal approach for hole placement—whether it should be situated at the extreme edge or introduced during the dicing process, which can potentially damage the structure. Significantly, uncertainty arises from the unknown capability of Deep Reactive Ion Etching (DRIE) to achieve the necessary length-to-width ratio crucial for wire accommodation and inclined sidewalls, given its specific use for high ratio etching. Furthermore, there is a need to evaluate the feasibility of depositing additional layers like photoresists to pattern the structure, particularly when the wafer already contains deep pre-existing holes.

3.2.1 Surface analysis of TiO2

Getting really smooth surfaces is key for processes like direct, anodic or ICB bonding. The quality of the bond relies heavily on how smooth the surfaces are in order to create a strong and dependable bond. They improve the contact between the bonding materials, reducing the chances of gaps or imperfections that could affect the bond. In processes like anodic bonding for instance, where voltage is applied, smooth surfaces make sure the electrical contact is consistent, resulting in a more efficient and stable bonding outcome.

'Rq' is a parameter used to characterize the surface roughness. It measures the root mean square of height deviations between points on the surface and a baseline (See Fig 4). In the context of microtechnology and magnetic sensor applications, the proposed intervals are as follows [5]:

- **Smooth:** $0.1\,\text{nm} \leq \text{Rq} < 1\,\text{nm}$
- **Moderately Smooth:** $1\,\text{nm} \leq \text{Rq} < 5\,\text{nm}$
- **Rough:** $5\,\text{nm} \leq \text{Rq} \leq 10\,\text{nm}$
- **Very Rough:** $\text{Rq} > 10\,\text{nm}$

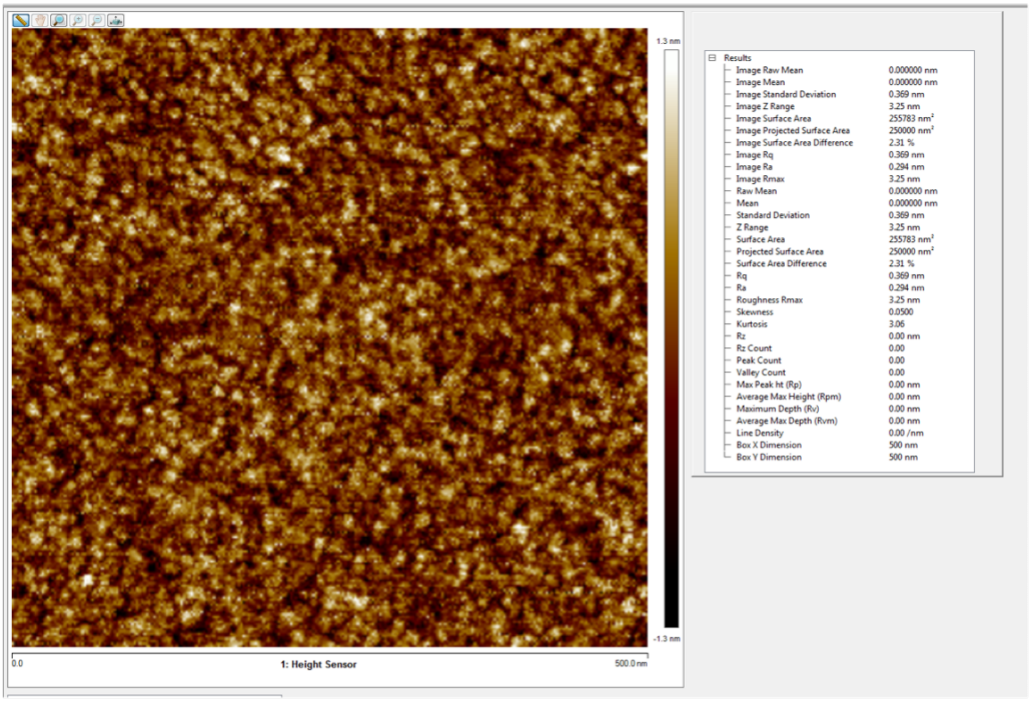


Figure 4: TiO2 surface AFM analysis

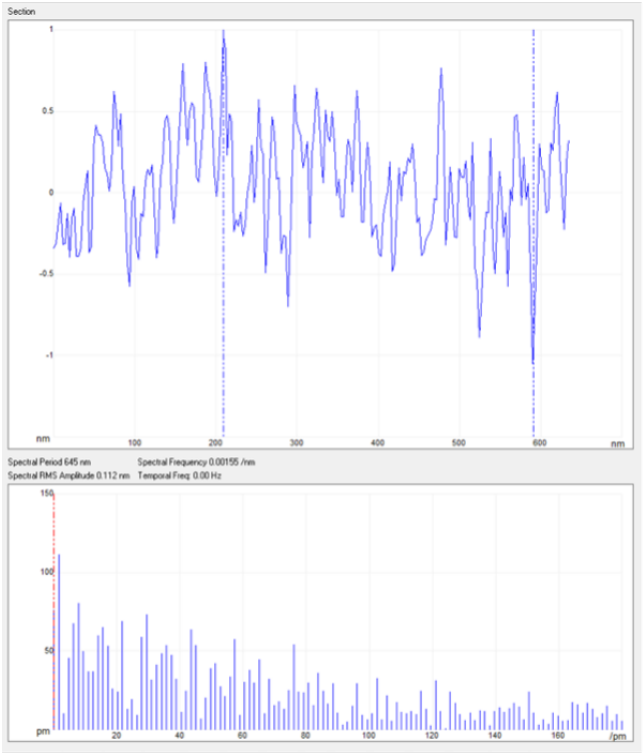


Figure 5: Surface Profile (Difference from highest point to lowest)

Consequently, it can be inferred that the layer is smooth and suitable for ICB bonding.

3.2.2 Simplification of tracks design and potential wires

(a) Design

In an effort to replicate the original tracks closely in terms of resistance, length, and specifications (same dd1, dd2, and ss1), Fig 6 illustrates the simplified design :

The process of determining the track length is straightforward; the total length is expected to be approximately 2 meters. The critical factor to ascertain is the number of iterations (n) for the tracks.

$$l = 2 \times 20 + 15.03 \times n$$

$$\Rightarrow n = \frac{l - 2 \times 20}{15.03} \approx 131$$

The resistance then is :

$$R = 9.79 \times 10^3\,\Omega$$

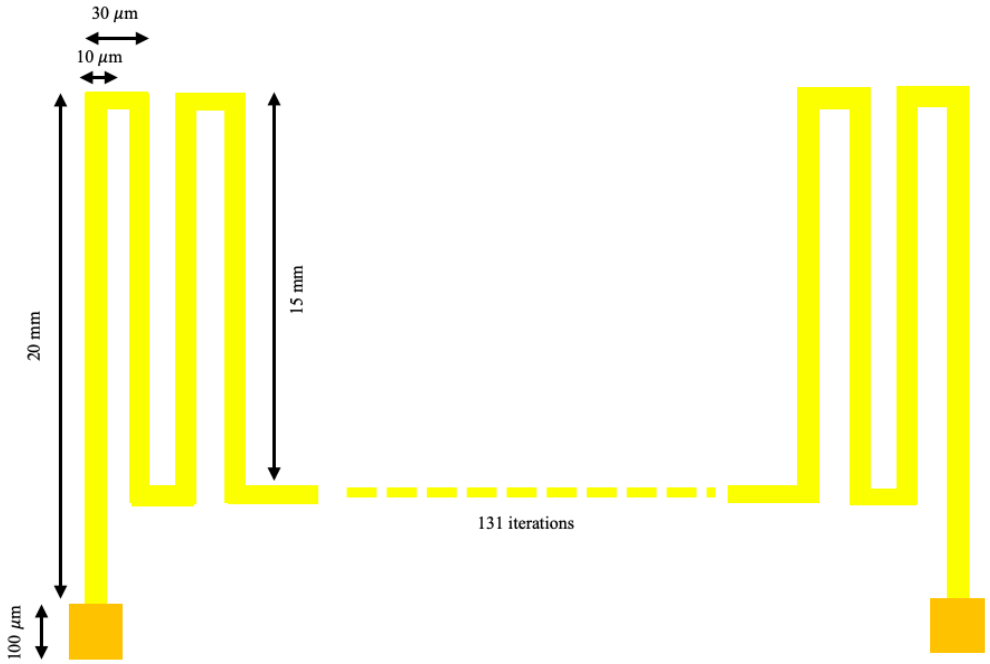


Figure 6: Simplified version of coil tracks

(b) Potential Wires

The selection of electrical wires for wafer bonding holds significance, with a key factor being the dimensions of the connection hole. An overview of standardized copper wires is provided below 7. Striking the right balance is essential, aiming for a minimal diameter to facilitate microfabrication and hole connection to the coil, while mitigating excessive resistance (inversely related to diameter). Recommended wires, falling within the 143um to 79.9um diameter range (identified as wires 35 to 40), offer resistances ranging from 0.0525 ohms to 0.167 ohms over a 5 cm length.

AWG	Diameter		Turns of wire, no insulation		Area	
	(in)	(mm)	(per in)	(per cm)	(kcmil)	(mm^2)
35	0.00561	0.143	178	70.1	0.0315	0.0160
36	0.00500*	0.127*	200	78.7	0.0250	0.0127
37	0.00445	0.113	225	88.4	0.0198	0.0100
38	0.00397	0.101	252	99.3	0.0157	0.00797
39	0.00353	0.0897	283	111	0.0125	0.00632
40	0.00314	0.0799	318	125	0.00989	0.00501

Figure 7: Overview of standardized copper wires

3.2.3 Use of Borosilicate as wafer material

The use of Borosilicate as wafer material has been proposed by M. Brun and IcoFlex engineers' team, especially Borofloat 33 (BF33) as it is very used in microelectronics for its good optical properties, high transparency in the visible and infrared spectra, as well as chemical and thermal resistance.

BF33 is a specific type of borosilicate glass, but due to the presence of boron, an application in the nuclear field would not be possible because it would not be stable, as indicated by this nuclear reaction:

$$^{10}_{5}\mathrm{B} + ^{1}_{0}\mathrm{n} \rightarrow ^{11}_{5}\mathrm{B} \xrightarrow{\text{decay}} ^{4}_{2}\mathrm{He} + ^{7}_{3}\mathrm{Li}$$

3.3 Process ideas

The decision was made to employ fused silica as the wafer substrate to mitigate the risk of a short circuit. Subsequently, various process variants were explored, encountering certain challenges. However, two primary approaches emerged: one involving the deposition of tracks followed by etching connection holes, and the other adopting the reverse sequence.

(a) **Etch connection hole, then deposit tracks**

The objective was to execute a photo-lithography process, starting with a Cr/Au mask due to the considerable depth of the DRIE and the necessity for robust protection of the pattern. Subsequently, a photoresist would be applied, exposed, and developed. The mask would undergo etching for the substrate, followed by DRIE etching. The standard process for tracks would then follow.

A potential bottleneck arises during the post-etching patterning of the tracks, especially concerning the application of photoresist onto the etched holes. The DRIE's high aspect ratio could impede the process.

While opting for this method might initially prove effective, it could pose challenges in future stages of the project, particularly when stacking coils becomes necessary. This could potentially create complications, making etching the connection hole first less than ideal.

(b) **Deposit tracks first, then etch connection hole**

In this process, the standard procedure involves depositing and burying the tracks. The intricacy lies in etching the connection holes without causing damage to the tracks and subsequently metallizing the area between them for the purpose of establishing connections. To achieve this, two photo-lithography steps are executed—one to etch the holes and another to establish connections with the tracks.

However, the challenge persists, particularly with the DRIE, which remains a potential complication in this scenario.

3.3.1 Exchanges with M. Hibert

M. Hibert is the team leader at CMi EPFL and has been a great help in the development of the final process flow.

He suggested avoiding DRIE, reasoning that the etch depth is not very substantial. Additionally, in this context, inclined sidewalls are needed for easier connections. Instead, he proposed employing a traditional wet etch in a 10% HF bath. This method can be done non-continuously, with the calculated etch time totaling 9 hours and 30 minutes, considering an etch rate of 175 nm/min, which offers the advantage of facilitating inspection.

Moreover, a prerequisite for a deep glass etching (>50 µm) is the utilization of a double-layer mask, comprising two layers of Cr/Au. This is imperative to prevent the emergence and expansion of "pinholes" beneath the masking layer. The formation of these pinholes is attributed to the elevated stress within the mask that can lead to the development of cracks and irregularities, potentially allowing the HF solution to permeate and resulting in the failure of the mask [3]. It is worth noting that the initial Chrome layer should possess greater thickness (50 nm) because gold has a propensity to diffuse at high temperatures. This diffusion may occur in the chrome and subsequently in the tracks, posing the risk of a short circuit.

He further advised employing thicker resists when coating the connection holes to ensure proper exposure. Following research and a comparison of available options, AZ125nXT emerged as a promising choice. According to the datasheet [1], this resist is well-suited for applications involving Through Silicon Via (TSV), plating, and RIE etching.

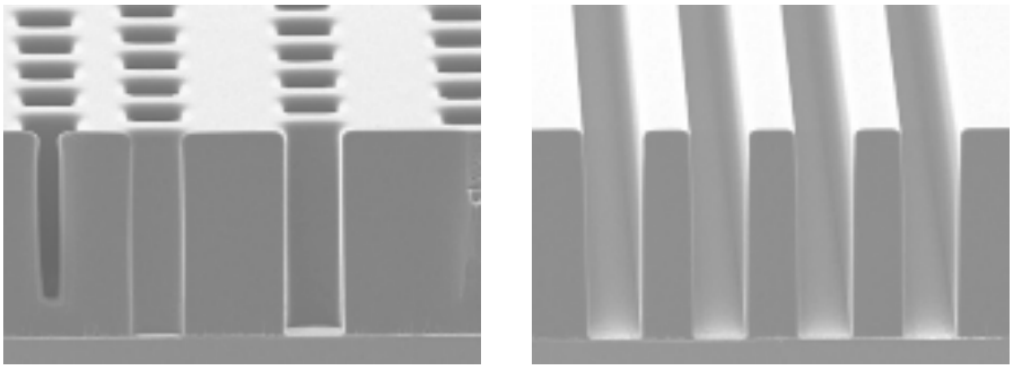
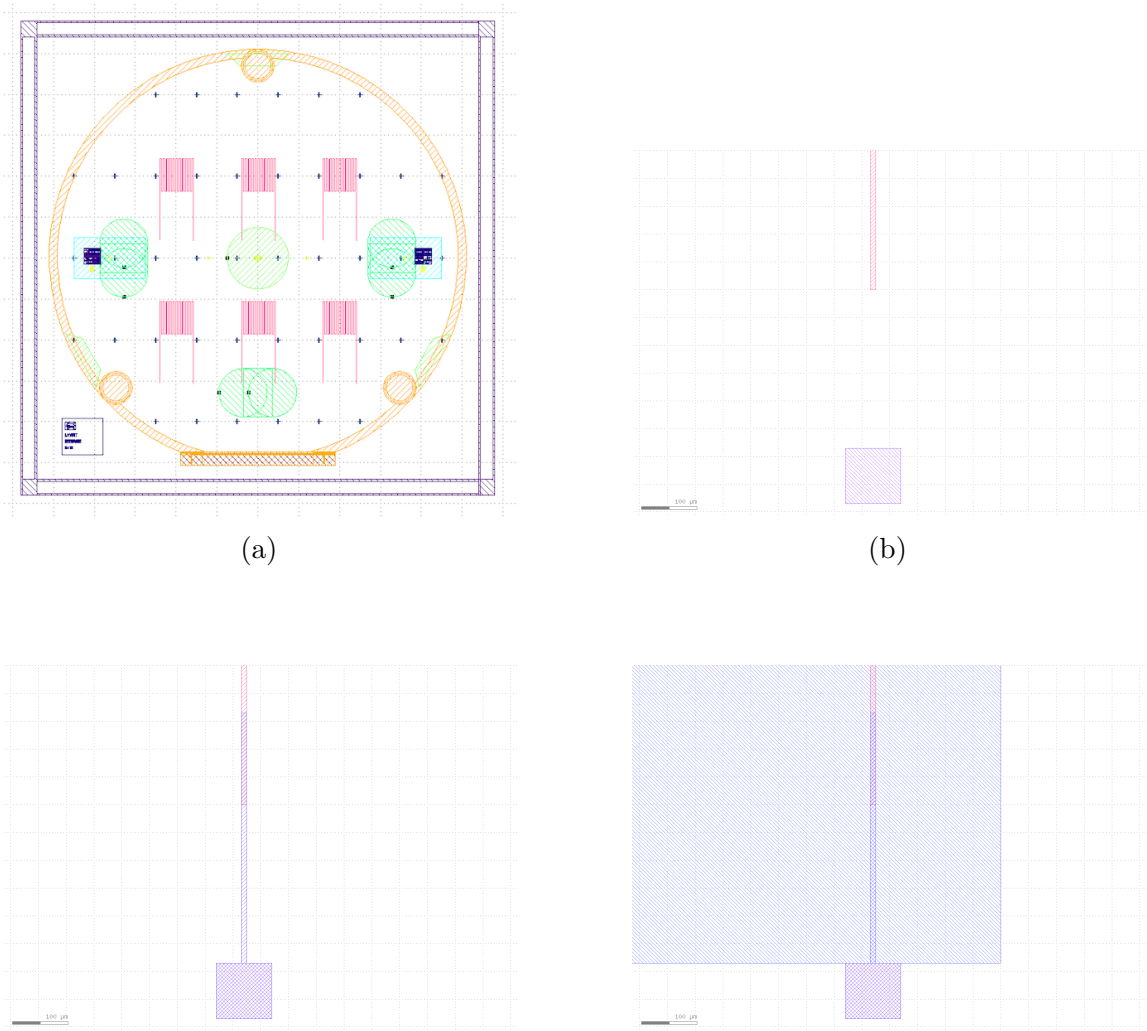


Figure 8: 15µm holes and 15µm lines in 70µm thick AZ 125nXT Cu substrate

4 Results and Next steps

Here are the 4 main steps for the process done on Klayout software:



(a) (b)

(c) (d)

Figure 9: 4 main steps with (a) deposition of tracks, (b) Connection hole wet etching, (c) Connection of both, (d) TiO2 layer deposition

The process flow, outlined in the appendices, provides a comprehensive overview of the entire procedure, elucidating the methodologies employed and detailing the materials utilized.

As shown in Fig 10, the hole has an approximate depth of 100 μm, with sidewalls inclined with an approximate angle of 45°.

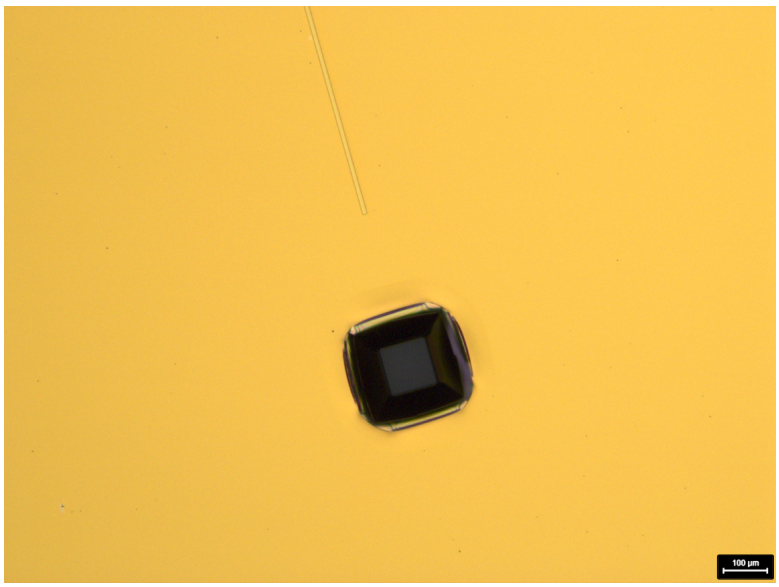


Figure 10: View of the deposited track and etched connection hole

While substantial progress was made in various aspects of the project, it is important to acknowledge some challenges encountered during the course of the work. Certain tasks could not be completed within the allotted timeframe, such as the connection with the tracks and the deposition of the TiO2 layer. These challenges, while impactful, have provided valuable insights for future considerations and improvements in similar endeavors.

The subsequent stages are well-defined and involve completing the process, conducting thorough inspections after each step to gather comprehensive data on potential issues. Simultaneously, collaborate with Mr. Brun on bonding experiments using diced wafers coated with TiO2 and Al2O3 (and possibly other materials) to validate the efficacy of ICB bonding. If issues arise, explore alternative options. Conclusively, bond the rudimentary "sensors" with their counterparts, and finally, delve into integrating the coils to achieve a finalized and resilient package.

An essential factor to consider, requiring a minor adjustment, is that the bonding occurs on the highest surface, which should be consistent wherever bonding takes place. In this scenario, and especially in the area indicated by the purple square in Figure 1, it is important that the tracks be buried and the connection hole closer.

Also, it is essential to be aware of the margins for etching in the burying process, ensuring that the deposition of tracks effectively fills the etched portion for a smooth surface. The same consideration applies to the absorption coefficients of radiation for various types of fused silica.

5 Conclusion

The journey of developing a robust packaging solution for DTT magnetic sensors has been both enlightening and challenging. The project aimed to enhance magnetic sensor design for fusion reactors, specifically the DEMO tokamak reactor. Throughout the process, collaboration and insights from experts played a crucial role in shaping decisions.

The exploration of microfabrication techniques, including the micro-coil design, resist choices, and surface analysis of TiO2, provided valuable insights into the intricacies of materials and methodologies. The exchanges with experts, notably M. Brun and M. Hibert, guided the project towards informed choices.

The inability to complete certain tasks within the allotted timeframe, such as connecting tracks and depositing the TiO2 layer, served as valuable lessons for future considerations.

Moving forward, the project outlines clear steps for completion, emphasizing thorough inspections after each stage, collaboration on bonding experiments, and the integration of coils for a finalized package. The importance of uniform bonding surfaces and optimal etching margins has been highlighted, providing specific directions for future work.

In conclusion, while certain challenges were encountered, the project lays the groundwork for advancing knowledge in materials processing for magnetic sensors in fusion reactors. The findings contribute to the broader goal of developing sustainable energy solutions and provide a foundation for future research in this domain.

6 Appendices

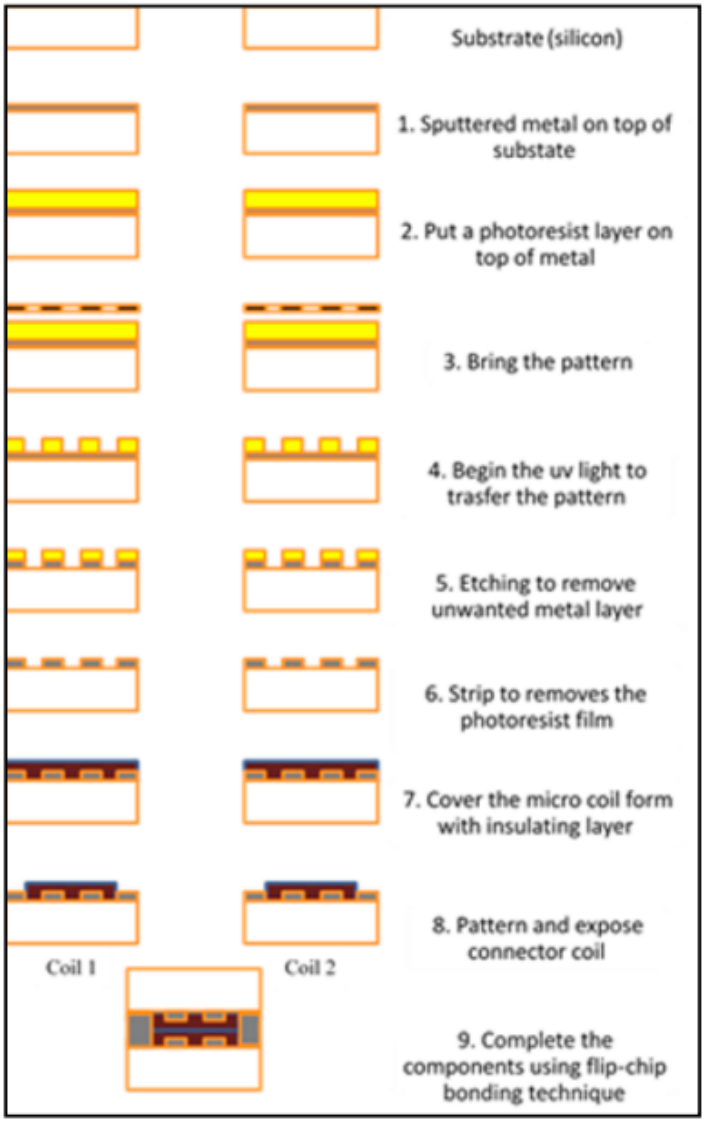


Figure 11: Process flow of the magnetometer's Surface Micromachining + Flip-Chip Bonding

6.1 Adapted process flow

Lab	Swiss Plasma Center	Phone	076 573 35 89
Operator Name	**Mehdi AMOR**	Office	-
Supervisor Name	Duccio TESTA	E-mail	mehdi.amor@epfl.ch
Date	06/12/2023		

CMi EPFL Center of MicroNanoTechnology

☑ Semestral Project ☐ Thesis ☐ Master Project ☐ Other

SPC Magnetic Sensor

Description of the fabrication project

Fabrication of conducting tracks (single layer) connected to a connection hole, with a layer of TiO2 deposited on tracks for wafer bonding

Technologies used
Evaporation, sputtering, Photolithography, lift-off, Wet etching, Dry etching, AFM

Ebeam litho data - Photolitho masks - Laser direct write data

Mask #	Critical Dimension	Critical Alignment	Remarks
1	**10 µm**	First Mask	Metal structuration
2	**100um**	20um	PR structuration
3	**200um**	10um	PR structuration
4	**20mm**	10um	PR structuration

Substrate type
Fused silica, Ø100mm, 525um thick, SiO_2: 100 %

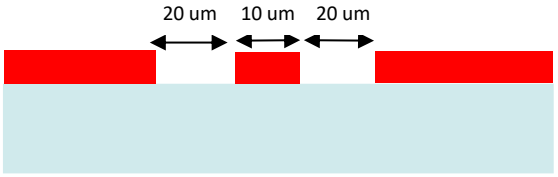
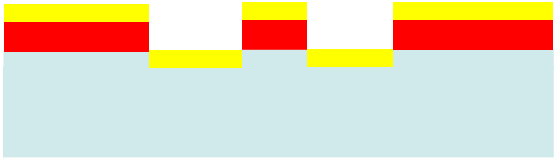
Interconnections and packaging of final device

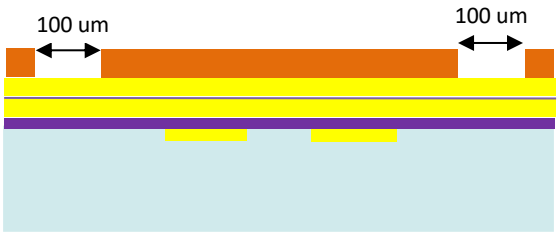
Thinning/grinding/polishing of the samples is required at some stage of the process.
☑ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.
☐ No ☑ Yes => confirm dicing layout with CMi staff

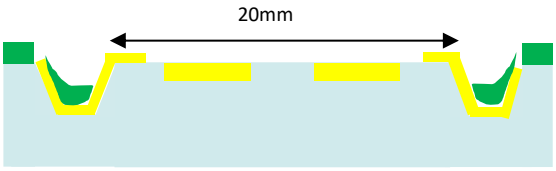
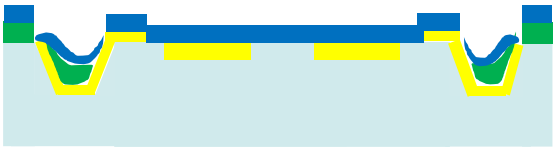
Wire-bonding of dies, with glob-top protection, is required at the end of the process.
☑ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

Step-by-step process outline

Step	Process description	Cross-section after process
00	***Substrate**: Fused Silica*	
01	***Cleaning*** *Machine: Piranha UFT wet bench*	
02	***Photolith PR coat*** *Machine: ACS200* *PR: AZ nLOF 2020 – 3 µm*	
03	***Photolith expo + develop*** *Machine: MLA150 and ACS 200*	
04	***PR stabilisation*** *Machine*: Oven 85°C, overnight	
05	***Dry etch*** *Material: SiO_2* *Machine: IBE* *Depth: 50 nm*	
06	***Metal Evaporation*** *Material*: Cr + Au *Machine*: EVA760 *Thickness*: 10nm + 40nm	

07	***Lift-off*** *Machine*: Plade Solvent	
08	***Two layers Sputtering*** *Material*: Cr + Au *Machine*: DP650 *Thicknesses:* ***First ->*** *50nm + 100nm* ***Second ->*** *10nm + 100nm* *Recipe: HTU_E60_300_Cr-Au-Cr-Au*	
09	***PR coating*** *Machine: ACS 200* *PR : AZ 10XT-07 – 1um* *Coating option: Dehydrate / EC*	
10	***Expo + development*** *Machine : MLA150 + ACS 200* *Recipe : D4_N_10XT_1u_PUD*	
11	***PR reflow*** *Machine : Dataplate (Z1)* *3 min @125°C*	
12	***Cr+ Au Etching*** *Machine : IBE* *Depth : 260nm*	

13	***SiO2 wet etching*** *Machine : Plade Oxide* *Depth : 100um* *Bath N°3 HF 10%* *Temperature: 40 °C* *Etching time: 9h31min (175nm/min)*	
14	***Photoresist stripping*** *Machine: Tepla 300 (Z11)* *1min @ high power* *+ Add remover1165*	
14bis	***Inspection*** *Machine: Bruker FastScan AFM*	
15	***Cr+ Au Etching*** *Machine : IBE* *Depth : 210 nm*	
16	***Cr wet etch*** *Machine: Arias Acid* *Depth: 50nm*	
17	***PR coating*** *Machine: Sawatec SM-200* *PR: AZ125nXT* *Thickness : 70um*	
18	***Expo + develop*** *Machine: MLA150 & Manuel development Arias Base* *Developer : AZ326 MIF*	

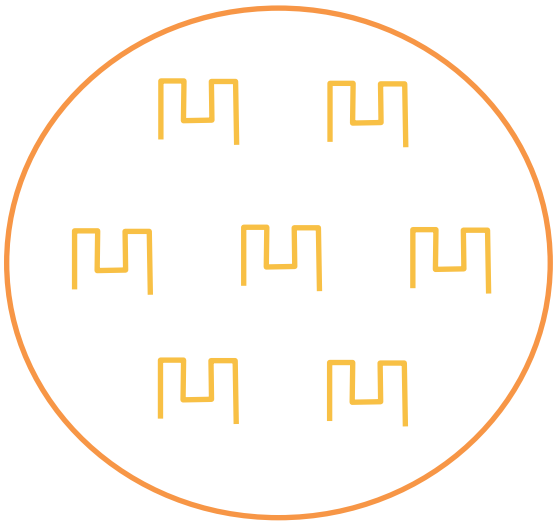
19	***O2 plasma descum*** *Machine: Tepla 300* *10s @ low power*	
20	***Evaporation*** *Material: Cr + Au* *Machine: EVA760* *Thickness: 10nm + 40nm*	
21	***Lift Off*** *Machine: Plade Solvent*	
22	***PR coating*** *Machine : Sawatec SM-200* *PR : AZ125nXT* *Thickness: 70um*	
23	***Expo + develop*** *Machine: MLA150 & Manuel development Arias Base* *Developer : AZ326 MIF*	
24	***O2 plasma descum*** *Machine: Tepla 300* *10s @ low power*	
25	***Sputtering*** *Material: TiO2* *Machine: DP 650* *Thickness: 50 nm*	

26	***Lift Off*** *Machine: Plade Solvent*	

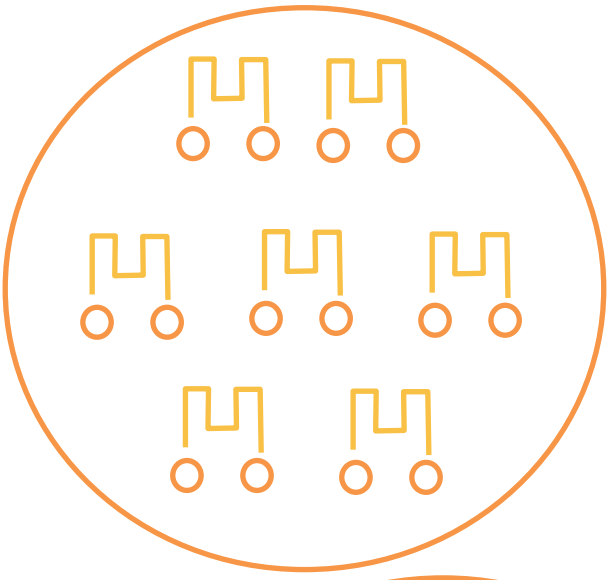
Annexes :

<u>Vues de haut</u>

1° Étape 7

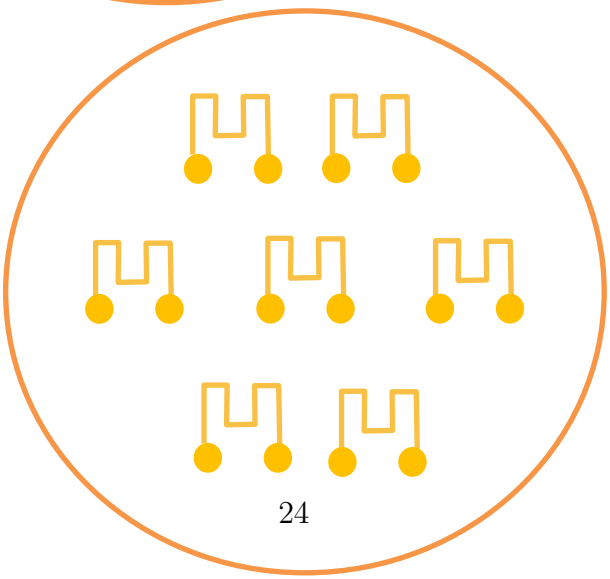


2° Étape 16

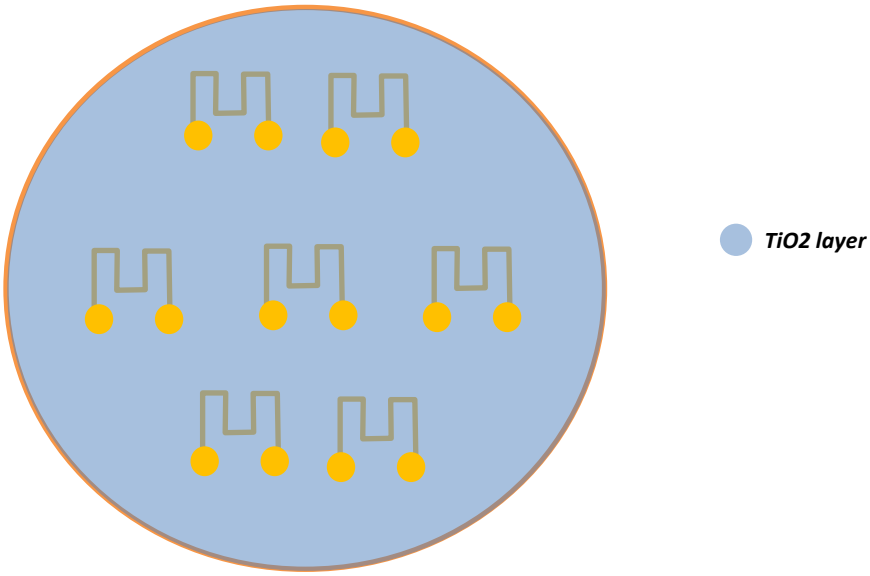


Trou de connexion

3° Étape 21



4° Étape 26



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